IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Y. Tanabe, et al.

Application No. Rule 53(b) of No. 10/355,301

Filed: April 12, 2004

For: FABRICATION PROCESS OF A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

Expected Examiner: G. Peralta

Expected Group: 2814

PRELIMINARY AMENDMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

April 12, 2004

Sir:

Please amend the above-identified application, prior to examination thereof, as listed in the following, and as set forth on the following pages:

Amendments to the Specification; and

Remarks are included following the amendments.